

<b>FORM PTO-1449</b> <b>U.S. DEPARTMENT OF COMMERCE</b> <b>PATENT AND TRADEMARK OFFICE</b>  <b>LIST OF REFERENCES CITED BY APPLICANT</b>  <i>(Use several sheets if necessary)</i>	<b>ATTORNEY DOCKET NO.</b> 826.1903	<b>APPLICATION NO.</b> 10/705,847
	<b>FIRST NAMED INVENTOR</b> Hiroyuki HIGUCHI	
	<b>FILING DATE</b> November 13, 2003	<b>GROUP ART UNIT</b> 2825

### U.S. PATENT DOCUMENTS


EXAMINER INITIAL		DOCUMENT NO.	DATE	NAME	CLASS	SUB- CLASS	FILING DATE
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						

### FOREIGN PATENT DOCUMENTS

		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB- CLASS	<u>TRANSLATION</u>	
							YES	NO
	AG							
	AH							
	AI							
	AJ							
	AK							
	AL							

### OTHER REFERENCES (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)

NND	AM	H. HIGUCHI, "An Implication-based Method to Detect Multi-Cycle Paths in Large Sequential Circuits", In Proceedings of the 39 <sup>th</sup> ACM/IEEE Design Automation Conference, pages 164-169, 2002.
NND	AN	K. NAKAMURA, et al., "Waiting False Path Analysis of Sequential Logic Circuits for Performance Optimization", IEEE/ACM ICCAD 98 pp. 392-395, 2002
NND	AO	S. DAVADAS et al., "Logic Synthesis", p. 236-241, McGraw-Hill, 1994

<b>EXAMINER</b> 	<b>DATE CONSIDERED</b> 02/13/2006
<small>EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.</small>	